IBM PowerPC 970
(a.k.a. G5)

Ref 1

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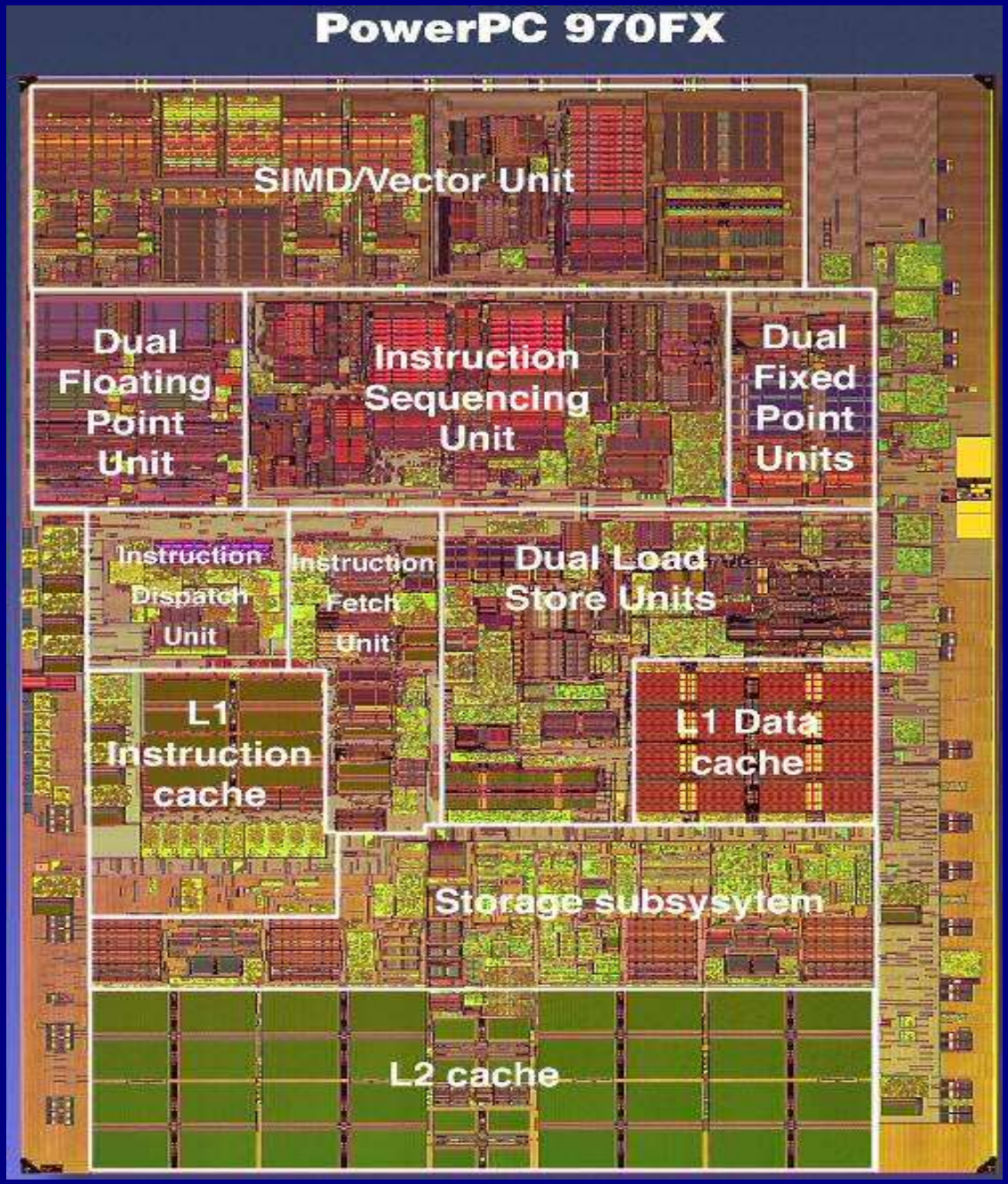
CS 466

PPC 970FX overview

- 64-bit RISC
- 58 million transistors
- 512 KB of L2 cache and 96KB of L1 cache
- 90um process with a die size of 65 sq. mm
- Native 32 bit compatibility
- Maximum clock speed of 2.7 Ghz
- SIMD instruction set (Altivec)
- 42 watts @ 1.8 Ghz (1.3 volts)
- Peak data bandwidth of 6.4 GB per second

A picture is worth a 2^10 words (approx.)

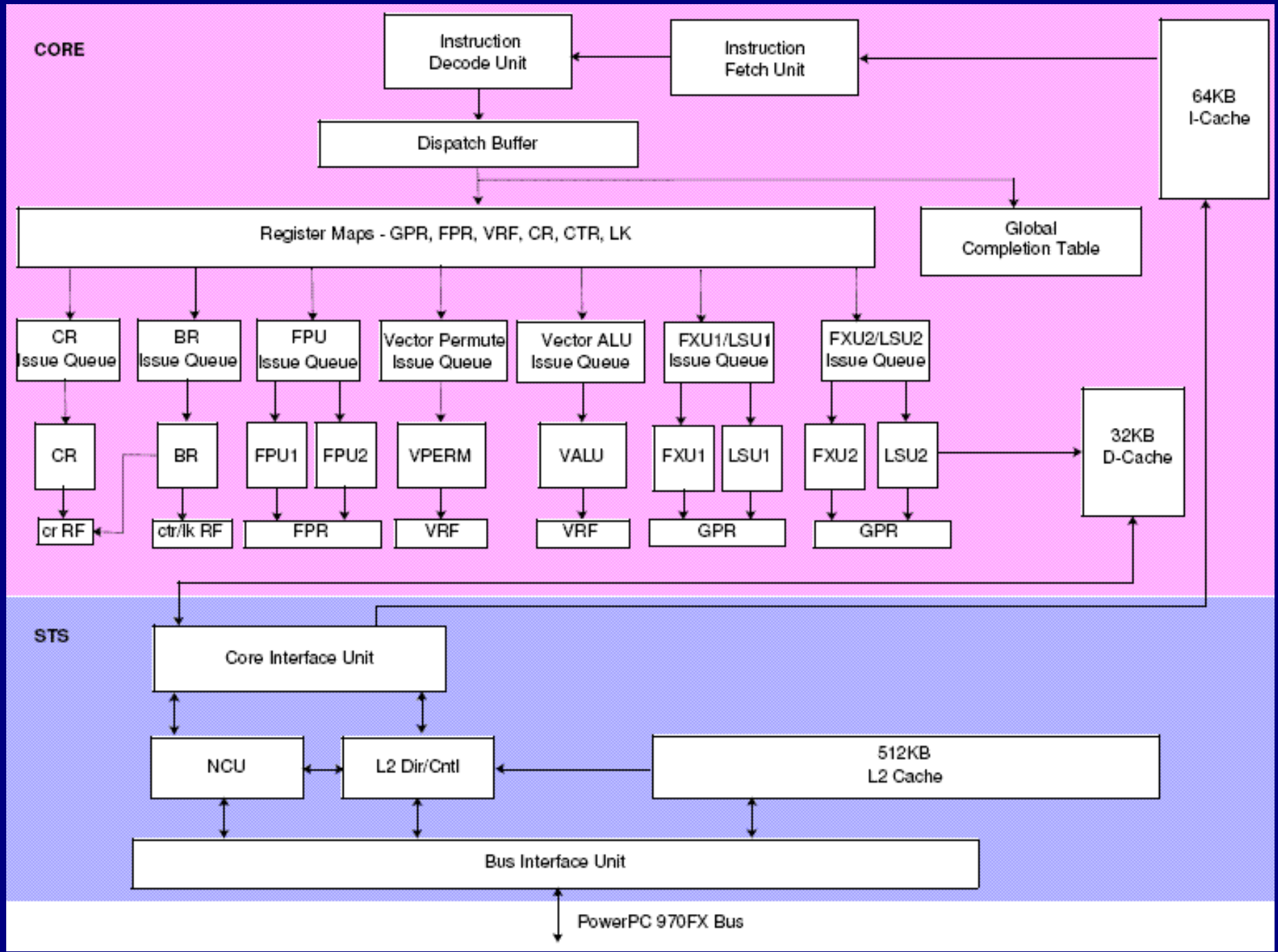


Ref 2

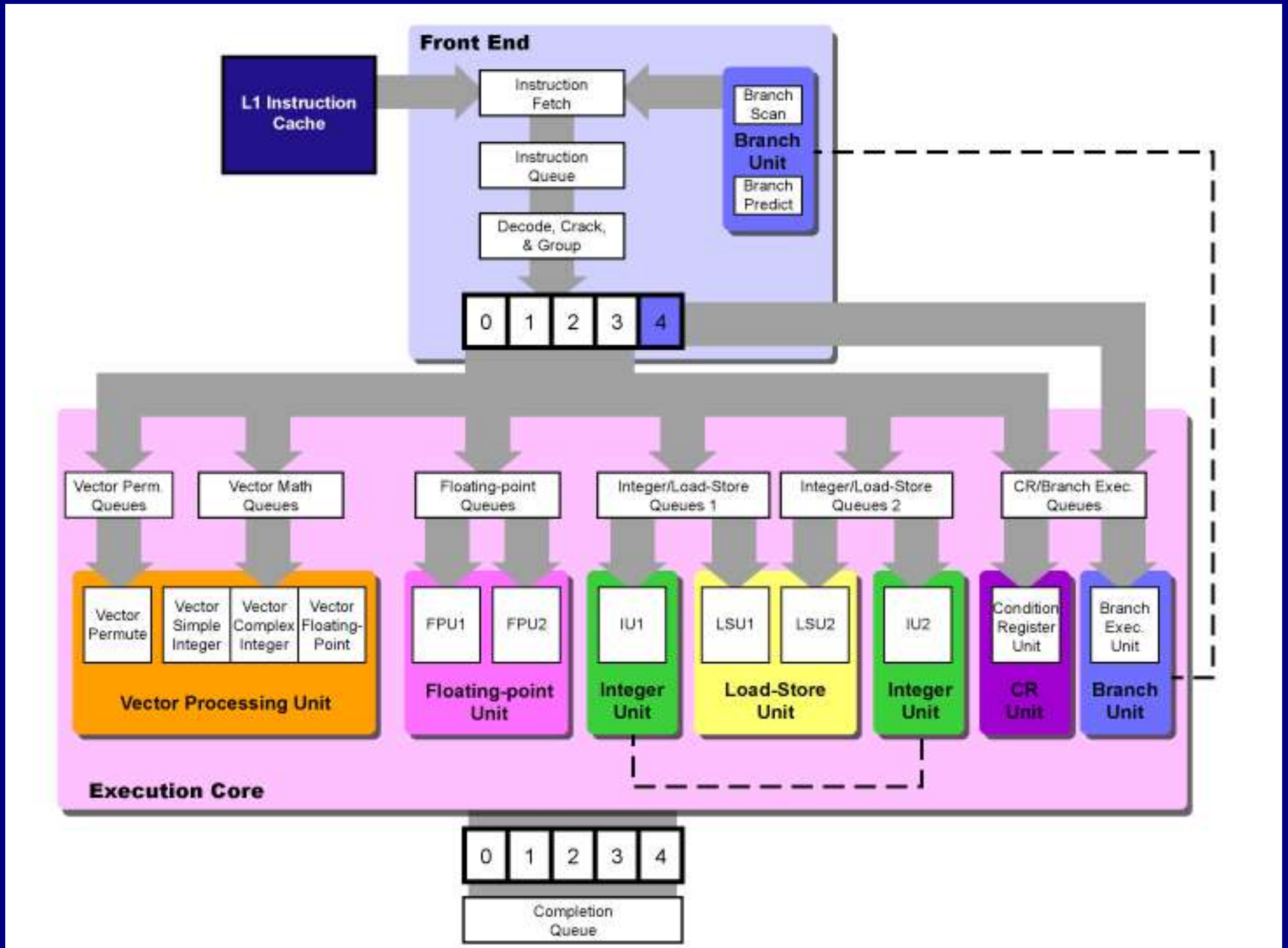
A little history

- PowerPC processor line is a product of the AIM alliance formed in 1991. (Apple, IBM, and Motorola)
- PPC 601 (G1) - 1993
- PPC 603 (G2) - 1995
- PPC 750 (G3) - 1997
- PPC 7400 (G4) - 1999
- PPC 970 (G5) - 2002
- AIM alliance dissolved in 2005

Processor



Ref 3


Front End
L1 Instruction Cache
Instruction Fetch
Instruction Queue
Decode, Crack, & Group
Branch Scan
Branch Unit
Branch Predict
0
1
2
3
4
Vector Perm Queues
Vector Math Queues
Floating-point Queues
Integer/Load-Store Queues 1
Integer/Load-Store Queues 2
CR/Branch Exec. Queues
Vector Permute
Vector Simple Integer
Vector Complex Integer
Vector Floating-Point
Vector Processing Unit
FPU1
FPU2
Floating-point Unit
IU1
Integer Unit
LSU1
LSU2
Load-Store Unit
IU2
Integer Unit
Condition Register Unit
CR Unit
Branch Exec. Unit
Branch Unit
Execution Core
0
1
2
3
4
Completion Queue

Ref 3

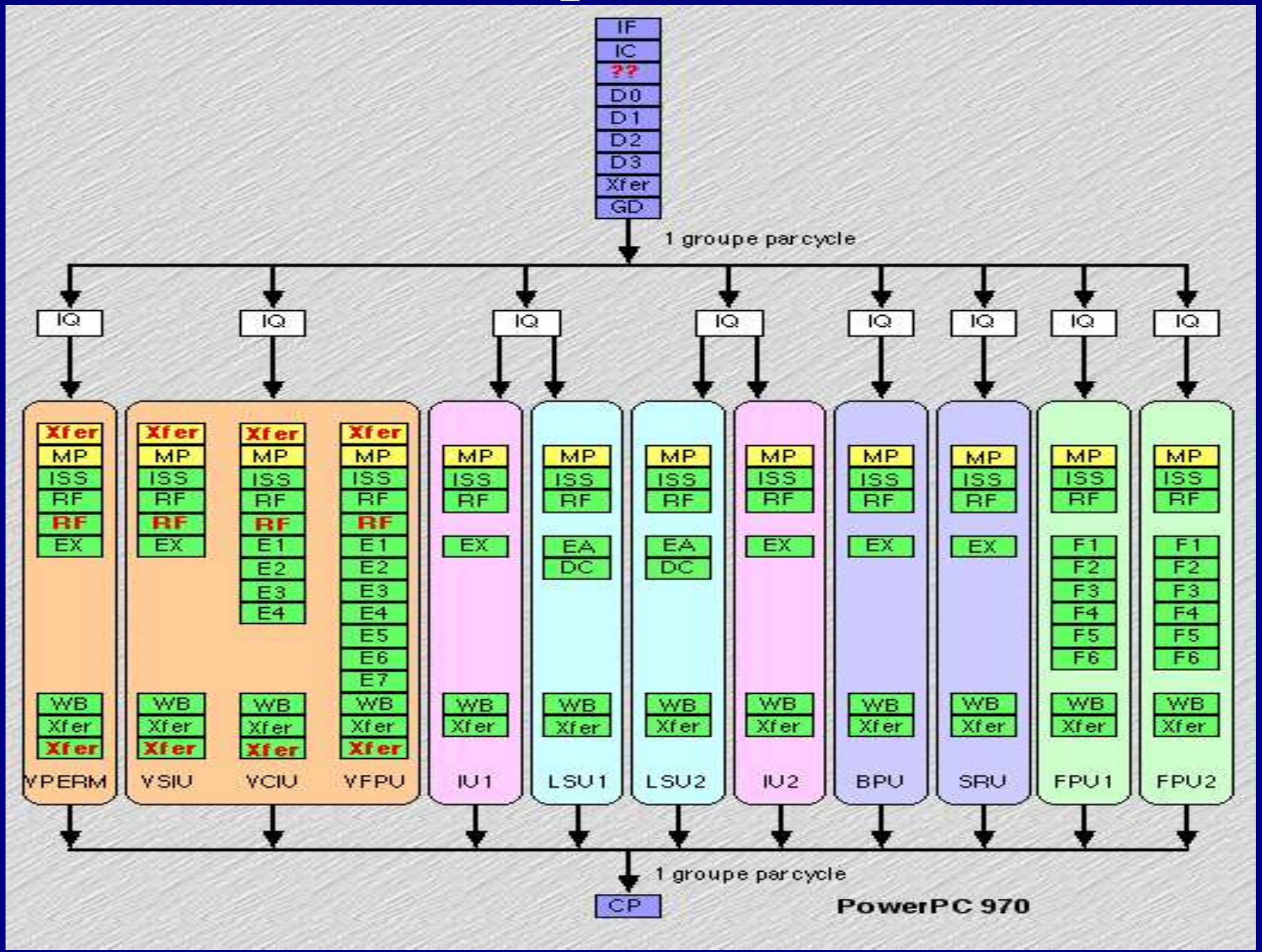
Core details

- 16(int)-25(vector) stage pipeline
- Large number of 'in flight' instructions (various stages of execution) - theoretical limit of 215 instructions
- 512 KB L2 cache
- 96 KB L1 cache
  - 64 KB I-Cache
  - 32 KB D-Cache

Core details continued

- 10 execution units
  - 2 load/store operations
  - 2 fixed-point register-register operations
  - 2 floating-point operations
  - 1 branch operation
  - 1 condition register operation
  - 1 vector permute operation
  - 1 vector ALU operation
- 32 64 bit general purpose registers, 32 64 bit floating point registers, 32 128 vector registers

Pipeline



Ref 4

Benchmarks

- SPEC2000
- BLAST – Bioinformatics
- Amber / jac - Structure biology
- CFD lab code

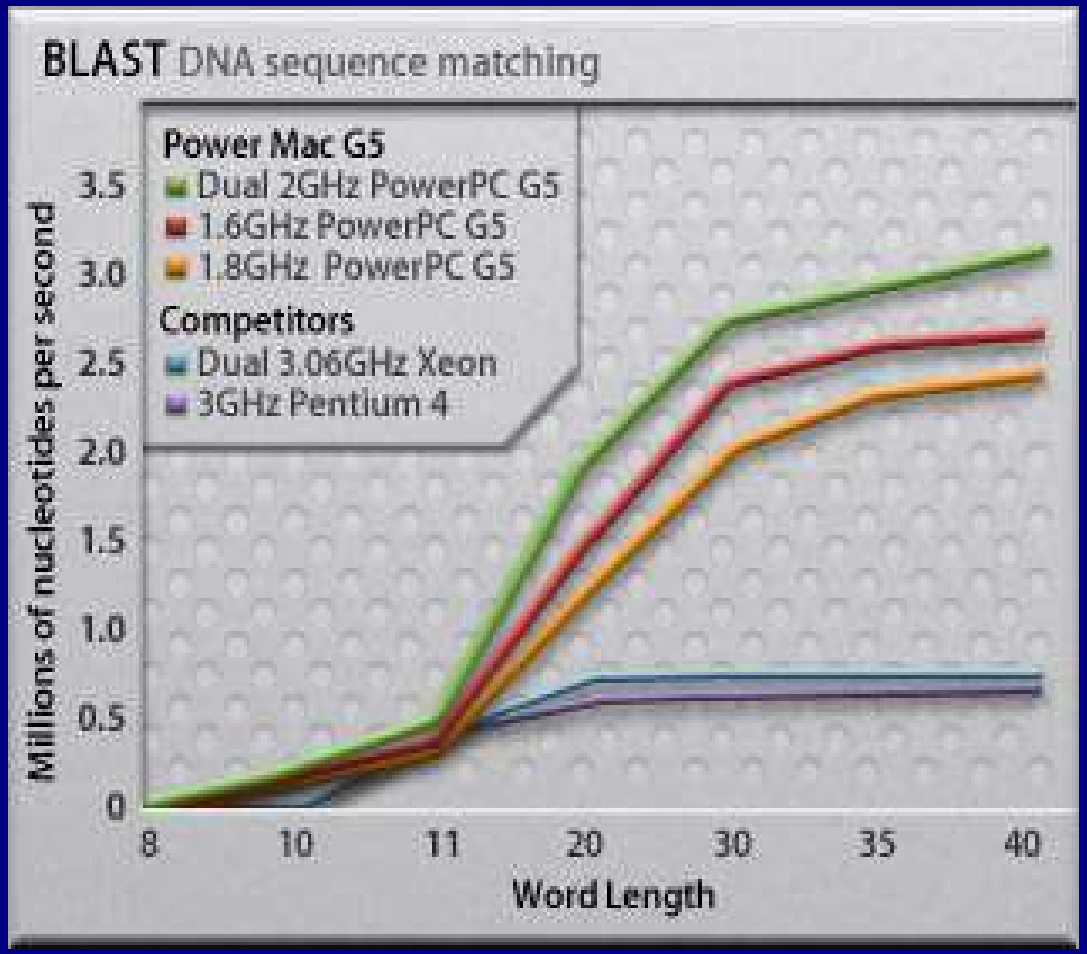
SPEC CPU2000

- IBM eServer BladeCenter JS20
- PPC 970 2.2Ghz
- SPECint2000
- Base: 986 Peak: 1040
- SPECfp2000
- Base: 1178 Peak: 1241

- Dell PowerEdge 1750 Xeon 3.06Ghz
- SPECint2000
- Base: 1031 Peak: 1067
- SPECfp2000
- Base: 1030 Peak: 1044

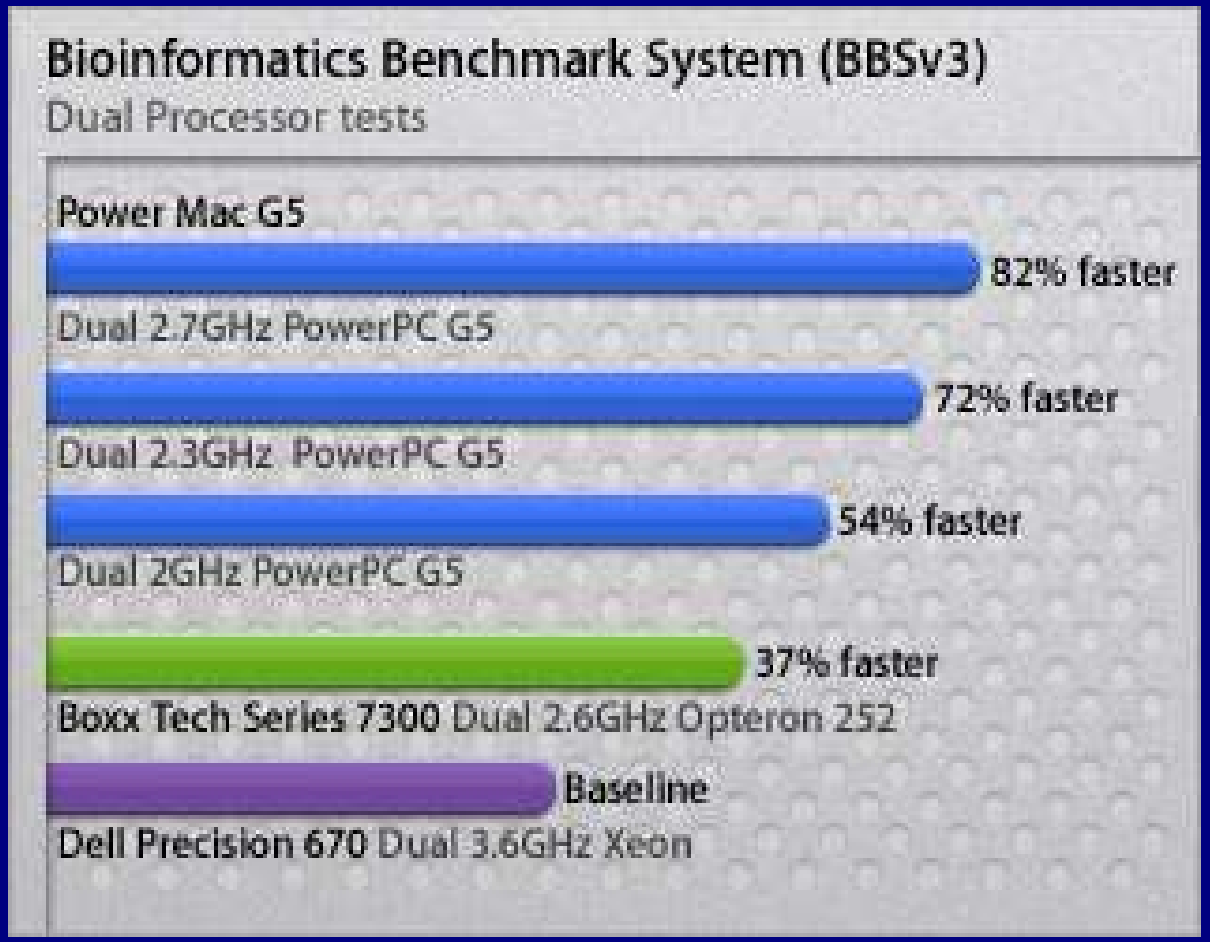
Apple's SPEC Results*2

BLAST


BLAST DNA sequence matching
Power Mac G5
Dual 2GHz PowerPC G5
1.6GHz PowerPC G5
1.8GHz PowerPC G5
Competitors
Dual 3.06GHz Xeon
3GHz Pentium 4
Millions of nucleotides per second
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0
8
10
11
20
30
35
40
Word Length

Ref. 5

BBSv3


Bioinformatics Benchmark System (BBSv3)
Dual Processor tests
Power Mac G5
82% faster
Dual 2.7GHz PowerPC G5
72% faster
Dual 2.3GHz PowerPC G5
54% faster
Dual 2GHz PowerPC G5
37% faster
Boxx Tech Series 7300 Dual 2.6GHz Opteron 252
Baseline
Dell Precision 670 Dual 3.6GHz Xeon

Ref. 6

Amber/jac

PME Simulation

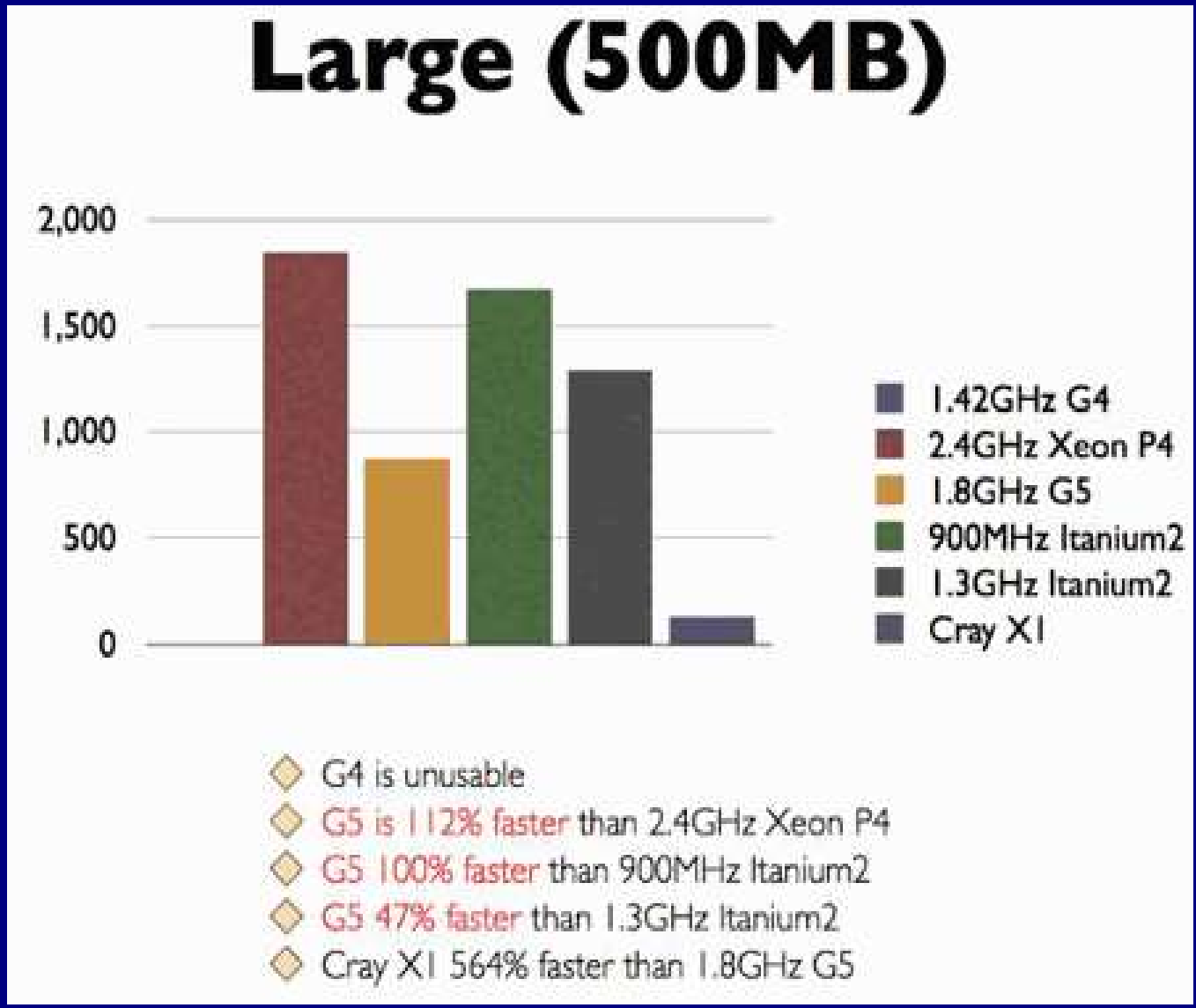
"jac" == Joint Amber/Charrm DHFR benchmark. This is the protein DHFR, solvated with TIP3 water, in a periodic box. There are 23,558 total atoms, and PME used with a direct space cutoff of 9 Ang. This is the benchmark in benchmarks/jac subdirectory of the Amber 7 distribution.

node-name	CPU	OS	compiler	npcu	time-per-step
PSSC Labs	Dual 2G Opteron	Linux	PathScale 1.0b3	1	0.700
PSSC Labs	Dual 2G Opteron	Linux	PathScale 1.0b3	2	0.360
PSSC Labs	Dual 2G Opteron	Linux	PGI 1.2.5	1	0.780
PSSC Labs	Dual 2G Opteron	Linux	Intel F90 7.1	1	0.720
Luo Lab	Dual 2.8G Xeon	Linux	Intel F90 7.1	1	0.934
Luo Lab	Dual 2.8G Xeon	Linux	Intel F90 7.1	2	0.675
Luo Lab	Dual 2.8G Xeon	Linux	Intel F90 7.1	4	0.576 (HTT)
Prof. E. M.	Dual 2G G5	MacOS X	XLF 8.1b	1	0.777

Ref. 7

CFD code

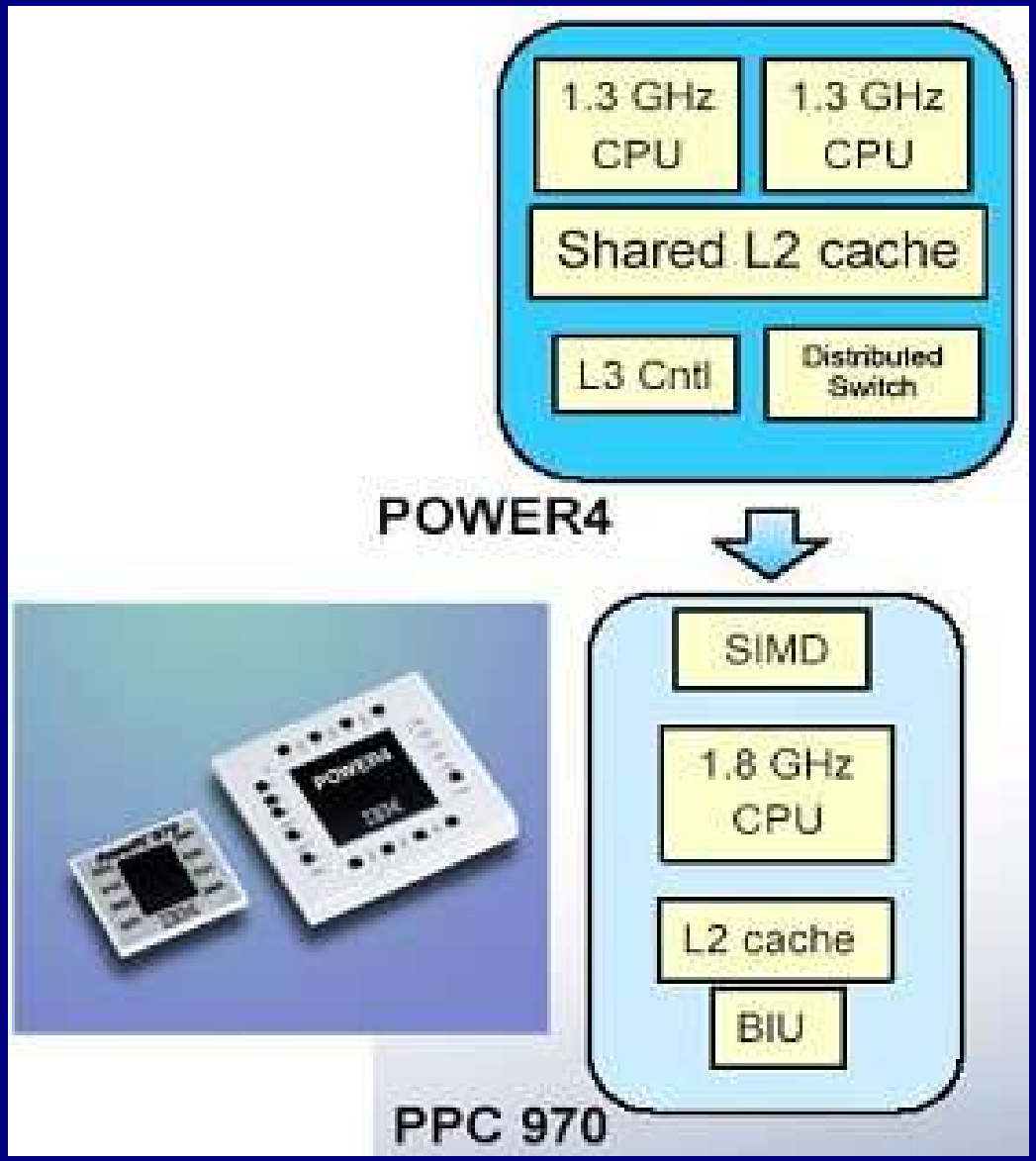
Prof. Sean Garrick, Dept. ME., Univ. of Minnesota



Ref. 8

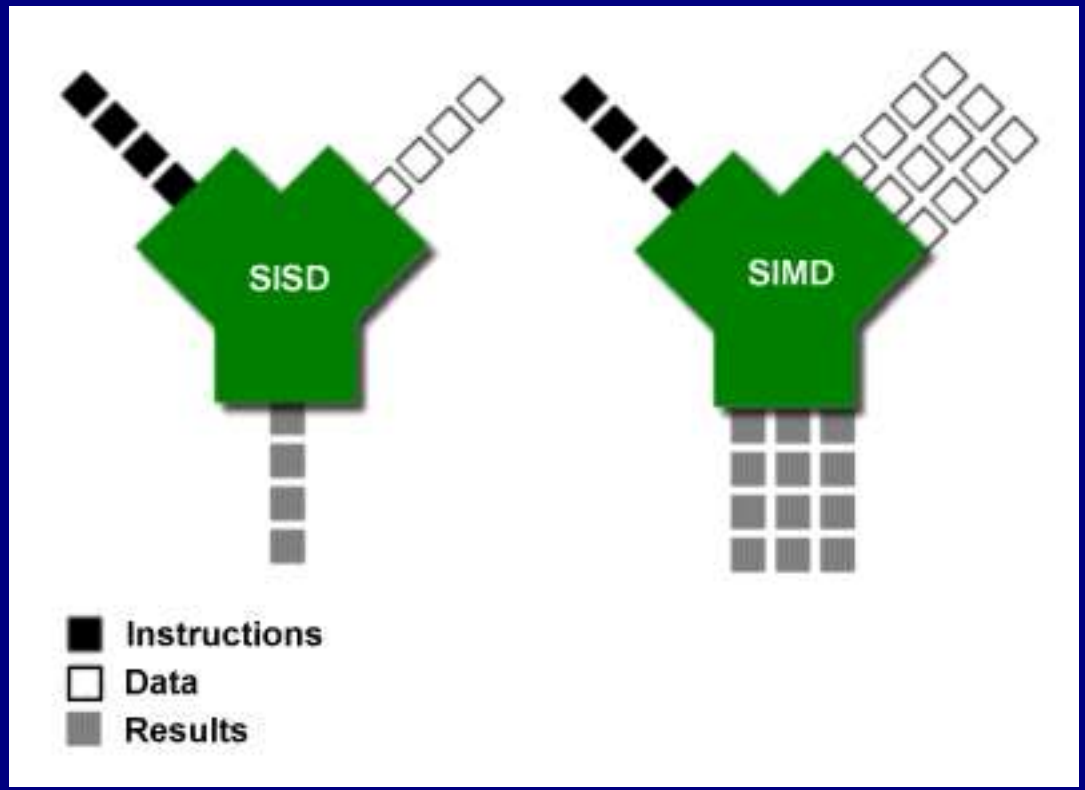
VMX

- PPC 970 = simplified Power4 + VMX
- a.k.a. Velocity Engine(Apple), AltiVec (Motorola)
- A vector processing add-on to PowerPC RISC instruction set
- Simple Instruction Multiple Data (SIMD)


1.3 GHz CPU
1.3 GHz CPU
Shared L2 cache
L3 Cntl
Distributed Switch
POWER4
SIMD
1.8 GHz CPU
L2 cache
BIU
PPC 970

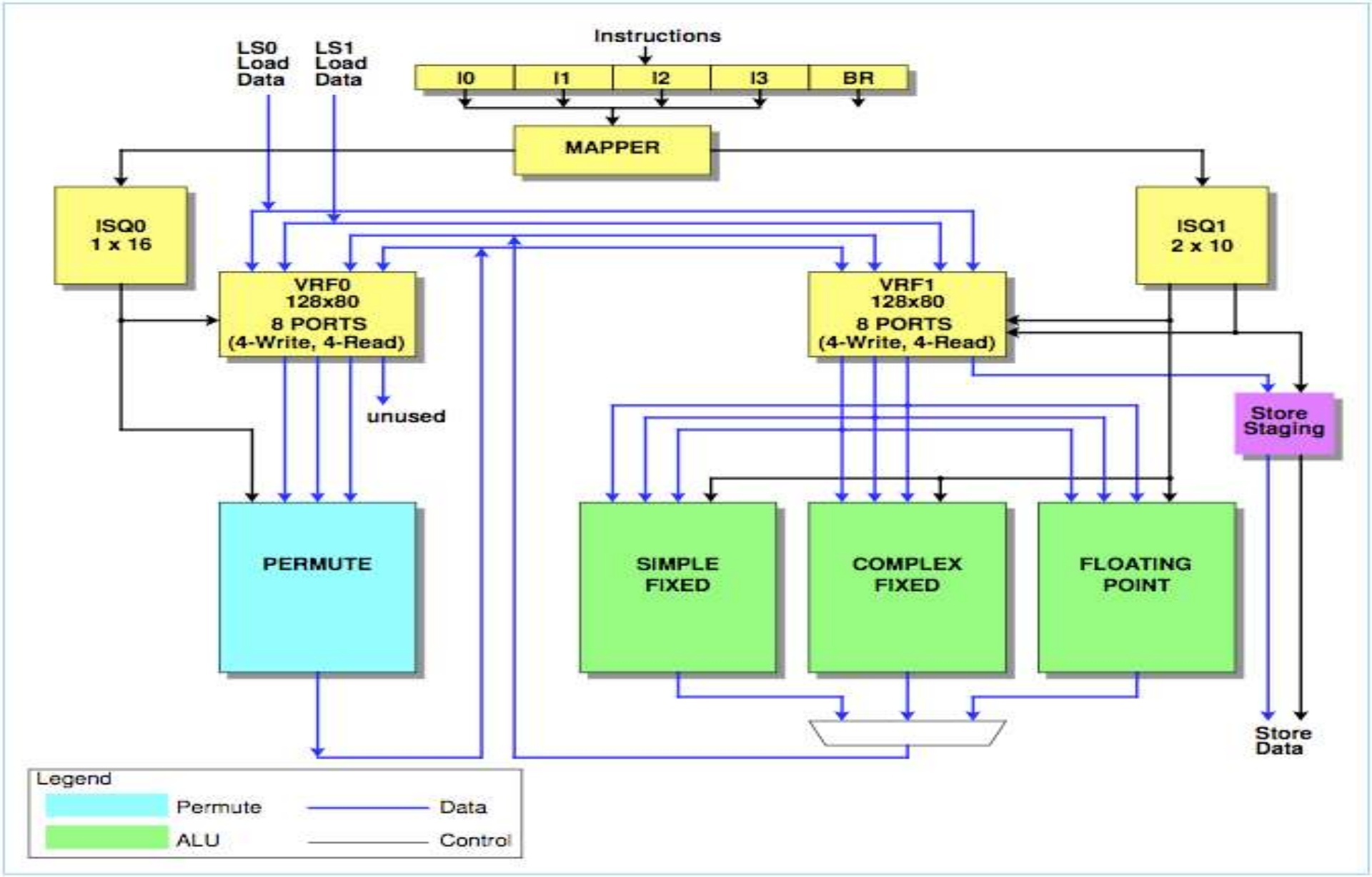
Single Instruction Multiple Data - SIMD

- SIMD vs. Instruction Level Parallelism
- Parallel in ‘Data’ vs. parallel in ‘instructions’



Ref. 9

Figure 12-1. VPU High-Level Block Diagram



Simple Code example

- 400Mhz G4, vector size: 1000
- Matrix addition (88 vs. 345 MFLOPS, 3.9X)
- Matrix rotation (300 vs. 472 MFLOPS, 1.6X)
- Matrix multiplication (84 vs. 384 MFLOPS, 4.6X)
- Apple's vector multiplication algorithm: up to 8X!

Applications

- Good for math, science and graphics manipulation
- Scientific array processing systems
- Muti-channel modems, echo cancelers, image and video processing system
- Internet routers

“Power Everywhere”

- POWER - Performance Optimization With Enhanced RISC
- 6 out of top10 in current top500 list are IBM RISC machines
- ps. Current No.5 is based on PPC970
- From high performance(supercomputer) to low power(embedded system)

“Power Everywhere”

- Power5
- Cell processor
- Power 970FX
- IP telephony, Internet modems, routers, game consoles
- Mars rovers: 32-bit RISC running VxWorks
- Expect more to come: Power.org

Questions?

References

1)http://www.macvillage.de/pages/x_magazin/ibmchips/Power970FX.jpg

2)www.anandtech.com/mac/showdoc.aspx?i=2436&p=2

3)IBM PowerPC 970FX RISC Microprocessor User's Manual

4)http://perso.wanadoo.fr/kakace/PowerPC/PPC970.html

5)http://www.spec.org/cpu2000/results/

6)http://www.apple.com/

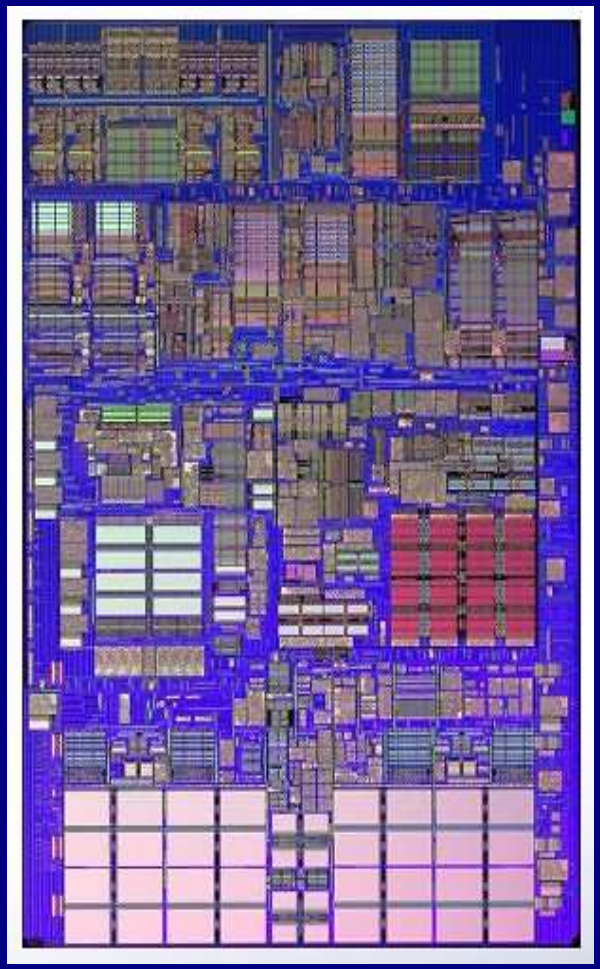
7)http://apple.sysbio.info/~mjhsieh/archives/000295.html

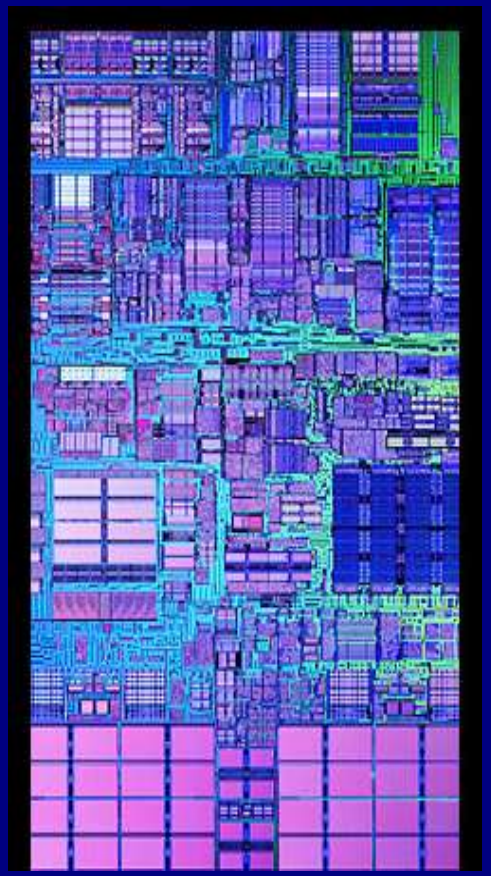
8)http://www.xlr8yourmac.com/G5/G5_fluid_dynamics_bench/G5_fluid_dynamics_bench.html

9)http://arstechnica.com/articles/paedia/cpu/simd.ars

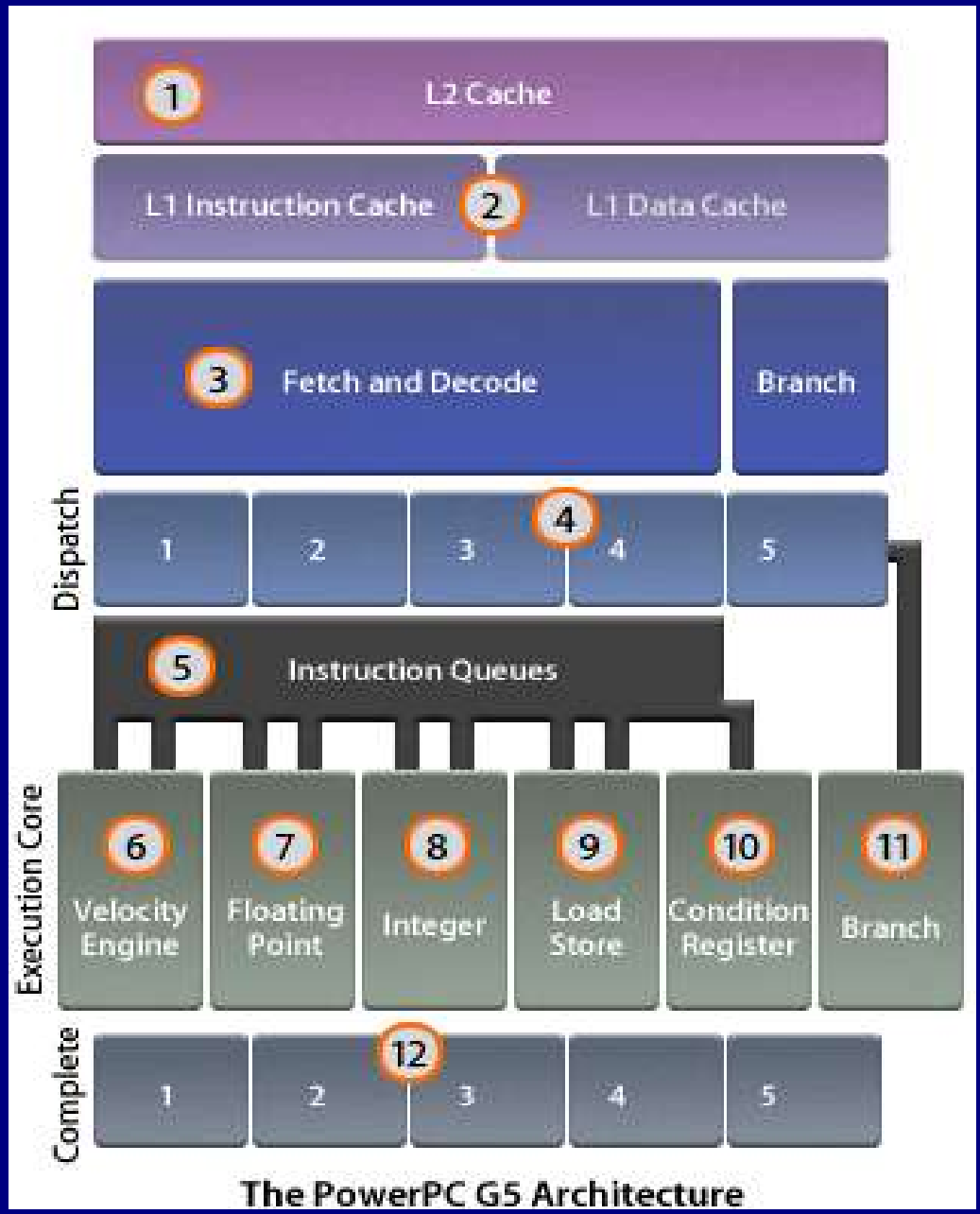
10)IBM PowerPC 970FX RISC Microprocessor User's Manual

Backup Slides






PowerPC 970FX
IBM



The PowerPC G5 Architecture

Execution Units

- Vector Permute Unit: 1-stage execution
  - Manipulate vector elements fast
- Vector ALU
  - Floating-point: 7-stages execution
  - Simple fixed: 1-stage execution
  - Complex fixed: 4-stages execution

Matrix Multiplication

$$\begin{bmatrix} c_{11} & c_{12} & \cdots & \cdots & c_{1n} \\ c_{21} & c_{22} & & & \vdots \\ \vdots & & \ddots & & \vdots \\ \vdots & & & \ddots & \vdots \\ \vdots & & & & \vdots \\ c_{n1} & \cdots & \cdots & \cdots & c_{nn} \end{bmatrix} = \begin{bmatrix} a_{11} & a_{12} & \cdots & \cdots & a_{1n} \\ a_{21} & a_{22} & & & \vdots \\ \vdots & & \ddots & & \vdots \\ \vdots & & & \ddots & \vdots \\ \vdots & & & & \vdots \\ a_{n1} & \cdots & \cdots & \cdots & a_{nn} \end{bmatrix} \begin{bmatrix} b_{11} & b_{12} & \cdots & \cdots & b_{1n} \\ b_{21} & b_{22} & & & \vdots \\ \vdots & & \ddots & & \vdots \\ \vdots & & & \ddots & \vdots \\ \vdots & & & & \vdots \\ b_{n1} & \cdots & \cdots & \cdots & b_{nn} \end{bmatrix}$$

$$c_{ij} = a_{i1}b_{1j} + a_{i2}b_{2j} + \cdots + a_{ik}b_{kj} + \cdots + a_{in}b_{nj}$$

In Scalar

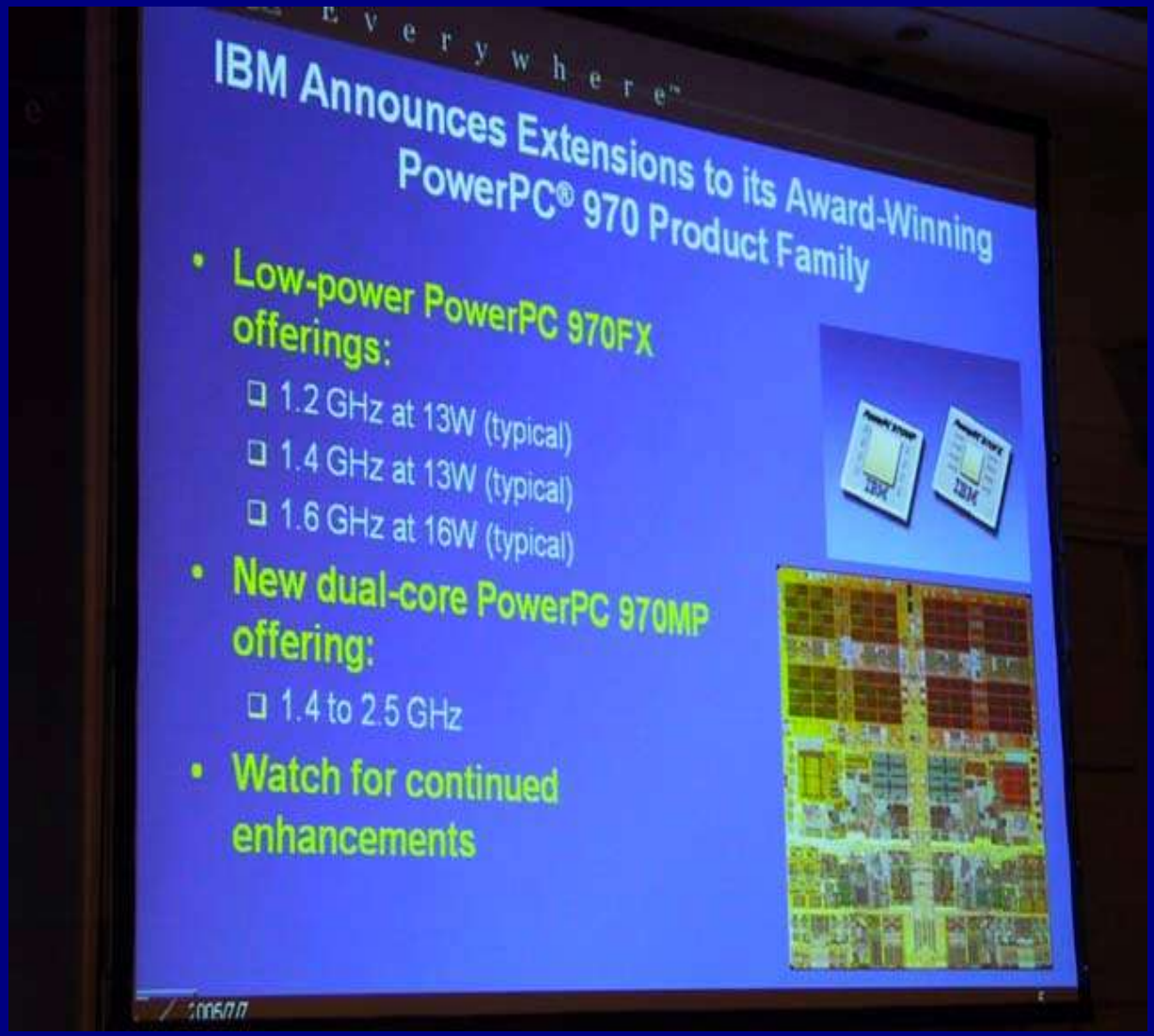
```
for (i=1, i<=n, i++) {
    for (j=1; j<=n; j++) {
        for (k=1; k<=n; k++) {
            c[i, j] = c[i, j] + a[i, k] * b[k, j];
        }
    }
}
```

In Vector

```
for (i=1; i<=n; i++) {
    for (j=1; j<=n; j++) {
        for (k=1; k<=n/4; k++) {
            c[ j+(i-1)*n ] = vector_madd(a[k+(i-1)*n],
                                         b[j+(k-1)*n],
                                         c[j+(i-1)*n];
        }
    }
}
```

References Continued

- http://ascii24.com/news/i/topi/article/2005/07/07/656844-000.html


Everywhere
IBM Announces Extensions to its Award-Winning PowerPC® 970 Product Family
• Low-power PowerPC 970FX offerings:
▫ 1.2 GHz at 13W (typical)
▫ 1.4 GHz at 13W (typical)
▫ 1.6 GHz at 16W (typical)
• New dual-core PowerPC 970MP offering:
▫ 1.4 to 2.5 GHz
• Watch for continued enhancements


Everywhere
Power Architecture™ Leadership
Scalability: from mW to GHz
Architecture Innovation
Power Architecture
Low Power
High Performance


Power Everywhere™
Aerospace
Mars Rovers: Spirit and Opportunity
Feature IBM's
Power Architecture™
Technology
High-performance 32-bit RISC
processor operates in high-radiation
space environment